ABSTRACT

A method of fabricating an integrated circuit having an n-channel and a p-channel transistor is provided. The method includes forming LDD regions for the n-channel transistors self-aligned to the gate electrodes. A first oxide is then formed over the structure and the n-type silicon regions are implanting with a p+ type dopant through the first oxide to form the source and drain regions of the p-channel transistor. A second oxide is formed over structure. The two oxide layers are then etched to provide sidewall spacers, having an inner portion formed from the first oxide and an outer portion formed from the second oxide. The p-type silicon regions are implanted with an n+ type dopant to form the low resistivity regions of the n-channel transistor. The p+ implants in the source and drain of the p-channel transistor typically outdiffuse toward the gates during further thermal processing of the device. The resulting integrated circuit has an LDD n-channel transistor and a p-channel transistor without an LDD region.